

REMARKS

Summary of Office Action

Claims 1-49 are pending in the above-identified patent application.

The Examiner has finally rejected claims 34 and 37-46 as being anticipated by Agrawal et al. U.S. Patent 6,097,212. Claims 35 and 36 have been objected to as being dependent from a rejected base claim, but allowable subject matter has been indicated. Claims 1-33, 47 and 48 have been allowed.

Summary of Applicants' Reply

Applicants note with appreciation the continued allowance of claims 1-33, 47 and 48, and the continued indication of allowable subject matter in claims 35 and 36. Applicants again hereby expressly reserve the right to rewrite either or both of claims 35 and 36 in independent form should the base claim ultimately not be allowed.

Request for Acknowledgment Of Drawing Correction

In the February 9, 2005 Office Action, the Examiner objected to FIG. 2 of the drawings. In their April 6, 2005 Reply to Office Action, applicants proposed an amendment of FIG. 2 of the drawings as required by the Examiner. Although the drawing objection is not repeated in the final Office Action, neither is applicants' proposed drawing amendment accepted or entered. Accordingly, applicants respectfully request that the Examiner acknowledge and enter the proposed drawing amendment submitted with the April 6, 2005 Reply to Office Action.

Summary of Telephonic Interview

The undersigned and the Examiner conducted a telephonic interview on May 3, 2005 to discuss the prior art rejection. The undersigned wishes to thank the Examiner for the courtesies extended during the telephonic interview. No agreement on the rejection was reached during the telephonic

interview, but the Examiner agreed to consider further argument.

Applicants' Reply to
The Prior Art Rejection

Claims 34 and 37-46 have been finally rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal. Claims 35 and 36 have been objected to as being dependent from a rejected base claim, but allowable subject matter has been indicated. The rejection and objection are respectfully traversed.

As previously indicated by applicants, claim 34 defines a multiplexer circuit that includes, in pertinent part, a number, L , of look-up tables, and a number, C , of control inputs, where $C = L+1$. The Examiner cites FIG. 11B of Agrawal as showing such a circuit.

Applicants respectfully submit that the structure shown in FIG. 11B of Agrawal does not meet the limitations of claim 34.

It must be remembered that claim 34 defines a multiplexer circuit. All of the other elements of the claim are characteristics of the multiplexer circuit. Thus for any reference to anticipate claim 34, the reference must show a multiplexer circuit having those limitations.

Specifically, claim 34 defines "[a] multiplexer circuit comprising: L look-up tables ... and C control inputs; wherein: $C = L+1$." Thus, as defined by claim 34, the number of control inputs of the claimed multiplexer circuit exceeds by one the number of look-up tables in the claimed multiplexer circuit.

Agrawal FIG. 11B shows a 4:1 multiplexer circuit 1100B having two look-up tables -- LUT 'a' and LUT 'b' ($L = 2$), as well as a 2:1 multiplexer for selecting between the output of LUT 'a' and the output of LUT 'b'. Because $L = 2$, for the reference to anticipate claim 34 it would have to show $L+1 = 2+1 = 3$ control inputs. Applicants and the Examiner differ on how many control inputs are shown in Agrawal FIG. 11B.

Both applicants and the Examiner agree that the control inputs are Select0 and Select1. However, because Select0 can be connected to both LUTs under the control of PIP₀, the Examiner considers Select0 to be two control inputs. Applicants respectfully disagree, because Select0 is only one signal, and even when it is connected to both of the LUTs, that connection is made under the control of PIP₀ which is part of the multiplexer circuit 1100B of FIG. 11B. Thus only two control signals are input into multiplexer 1100B. The fact that PIP₀, itself a component of multiplexer 1100B, can be set to reuse one of the control inputs does not increase the number of control inputs to multiplexer 1100B.

The text describing Agrawal FIG. 11B supports applicants' position:

Referring to FIG. 11B, a third decoding mode is referred to herein as the 4:1 MUX-emulating mode. In this third mode, PIP₀ is activated (to make a connection) while PIP₁ and PIP₂ are each deactivated. POP₃ is activated (to make an opening between MIL# 4 and line 1140). In one variation of this third decoding mode, LUT's 'a' and 'b' are configured to behave as 2:1 multiplexers with lines 1130 and 1140 being the respective selection control lines. These lines 1130 and 1140 are strapped together by the activated PIP₀ to define a Select0 control line of a 4:1 multiplexer. MIL# 4 (1150) becomes the Select1 control line of the 4:1 multiplexer as shown while MIL's 2, 3, 5 and 6 define desired ones of inputs In₀, In₁, In₂ and In₃ of the illustrated 4:1 multiplexer.

(Column 53, lines 1-13; emphasis added.) Thus, the text of the reference itself teaches that the inputs to the two LUTs are strapped together to form "a Select0 control line" -- i.e., a single control line. The Examiner cannot substitute his own interpretation for the plain teaching of the reference.

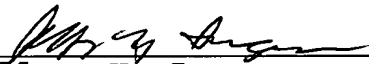
It is incontrovertible, then, that FIG. 11B of Agrawal shows a multiplexer circuit 1100B with only two control inputs, or in other words in Agrawal $C = 2 = L \neq L+1$. Thus, Agrawal does not show or suggest the claimed invention.

Accordingly, applicants respectfully submit that claim 34 is not anticipated by Agrawal and is patentable. Each of claims 35-46 depends, directly or indirectly, from claim 34, and accordingly each of claims 35-46 is patentable as well.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application is in condition for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

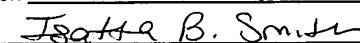
Respectfully submitted,

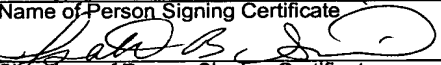


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